## REMARKS

*Claim Rejections Under 35 U.S.C. § 102*

Claims 1-3, 5, 11, 12, 15, 18 and 21 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Baltz et al.* (U.S. Patent No. 6,058,474). Applicant respectfully traverses this rejection.

Claims 1, 6, 11, 16, 19, 20, and 21 have been amended to add limitations that illustrate the connections between the memory devices and the processor. The limitations are to the separate buses between each of the non-volatile memory and the processor and the volatile memory and the processor. Limitations have also been added that illustrate the dedicated bus between the two memories.

*Baltz et al.* discloses using DMA circuitry 100 to transfer data from an 8-bit EPROM 671 to internal program memory 23 as is illustrated in Figure 8. Applicant's invention, as claimed in the amended claims, does not require such intervention. Data from non-volatile memory is transferred directly to volatile memory over a dedicated bus that connects only those two memories. The transfer is independent of the processor or any DMA circuitry. Additionally, the non-volatile memory of the present invention is coupled to the processor separately from the volatile memory unlike the circuitry in *Baltz et al.* Therefore, Applicant's invention as claimed in the amended claims is neither taught nor suggested by *Baltz et al.*

*Claim Rejections Under 35 U.S.C. § 103*

Claims 4, 6-9, 14, 16-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Baltz et al.* in view of *Harari et al.* (U.S. Patent No. 6,266,724). Claim 13 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Baltz et al.* in view of *Shin et al.* (U.S. Patent No. 6,735,669). Claims 10 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Baltz et al.* in view of *Harari et al.* as applied to claims 6 and 19, and further in view of *Shin et al.* Applicant respectfully traverses these rejections.

Applicant's claimed invention is to a system with volatile memory coupled to a processor over a synchronous first bus and a non-volatile memory coupled to the processor over a serial second bus. The two memories are directly connected over a dedicated third bus that connects

only the memories. Even if it were obvious to combine the cited references, and Applicant maintains that it is not, no combination of *Baltz et al.*, *Harari et al.*, and/or *Shin et al.* would teach or suggest Applicant's invention as claimed in the amended claims.

## CONCLUSION

For the above-cited reasons, Applicant respectfully requests that the Examiner withdraw the final rejection and allow the claims of the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

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